REMARKS

Claims 1-42 are pending in the application.

Claims 1-16 and 22-37 are rejected using new grounds.

Claims 17-21 and 38-42 would be allowable if rewritten to overcome the rejections under *35 U.S.C. § 112*, second paragraph, and including all of the limitations of the base claim and any intervening claims. The Applicants thank the Examiner for allowing these Claims.

The Applicants respectfully assert that the amendments to Claims 5-7, 12, 26-28, and 33 and incorporated by reference in any claims depending therefrom, are not narrowing amendments made for a reason related to the statutory requirements for a patent that will give rise to prosecution history estoppel. *See Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S. Ct. 1831, 1839-40, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 234 F.3d 555, 566, 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2001).

I. EXAMINER INTERVIEW

The Applicants had a telephone conversation with Examiner Tan on February 4, 2005 to discuss the prior art reference *Kim* cited for the rejections. The Applicants conveyed to the Examiner the difficulty in understanding what *Kim* is teaching in his invention. The Applicants explained that while *Kim* does have some elements similar to the present invention, their interconnection and function are not the same. The Examiner stated that he would carefully review the Applicants' arguments in light of our concern that *Kim* is not explained very clearly. It is the Applicants' contention that one of ordinary skill in the art would have great difficulty using the invention of *Kim* as the details of how he selects his terminator elements are not disclosed.

II. CLAIM OBJECTIONS

The Examiner objected to Claims 9 and 10 because he asserts that the negative input of receiver/comparator 204 is shown coupling to Vref in FIG. 2 whereas the claims recite coupling to the threshold voltage. The Applicants assert that the Specification, page 6, lines 18-20 describing FIG. 2 states: "A receiver 204 is also coupled to common terminal 203 and detects signals on common terminal 203 by comparing the signals relative to threshold voltage Vref 222 generating a detected signal at output 262." It is clear that Vref 222 is the threshold voltage. Therefore, the Applicants respectfully assert that the objection to Claims 9 and 10 because of the above informalities is traversed for the above reasons.

II. REJECTION UNDER 35 U.S.C. § 112

The Examiner rejected Claims 5-7 and 26-28 under *35 U.S.C. § 112*, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which the Applicants regard as the invention.

The Applicants have amended Claims 5 and 26 changing "first" in line one to "second." This changes the first termination network to the second termination network which is coupled in response to the first and second control signals. Therefore, the Applicants respectfully assert that the rejections of Claims 5 and 26 under *35 U.S.C. § 112*, second paragraph, are traversed with the above noted amendments.

The Applicants have amended Claims 7 and 28 changing "third" in line one to "first." This changes the third termination network to the first termination network which is coupled in response to the fifth and sixth control signals. Therefore, the Applicants respectfully assert that the rejections of Claims 7 and 28 under *35 U.S.C. § 112*, second paragraph, are traversed with the above noted amendments.

The Applicants have amended Claims 6 and 27 changing "second" in line one to "third." This changes the second termination network to the third termination network which is coupled in response to the third and fourth control signals. Claim 6 has also

been amended to correctly depend from Claim 3 to correct the antecedent basis problem. Likewise, Claim 27 has been amended to correctly depend from Claim 24 to correct the antecedent basis problem. Therefore, the Applicants respectfully assert that the rejections of Claims 6 and 27 under *35 U.S.C. § 112*, second paragraph are traversed with the above noted amendments.

The Examiner rejected Claims 12-16 and 33-36 under *35 U.S.C. § 112*, second paragraph, as being indefinite for failing to point out and distinctly claim the subject matter which the Applicants regard as the invention. The Examiner states that Claims 12-16 and 33-36 recite the limitation "TL" which has no antecedent basis. The Applicants have amended Claims 12 and 33 to show that "TL" is short for transmission line as suggested by the Examiner. Therefore, the Applicants respectfully assert that the rejections of Claims 12-16 and 33-36 under *35 U.S.C. § 112*, second paragraph are traversed with the above noted amendments.

III. REJECTION UNDER 35 U.S.C. § 102(e)

The Examiner rejected Claims 1-4 and 8-10 under *35 U.S.C. § 102(b)* as being anticipated by U.S. Patent No. 6,556,038 to *Kim et al.* (hereafter "*Kim*").

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

The Examiner states that *Kim* teaches all the claimed limitations of Claim 1 in Figs. 5-10. The Examiner states that *Kim*'s receiver 20 teaches the receiver of Claim 1. The Examiner then states that network 30 of *Kim* teaches the termination network of Claim 1. The termination network of Claim 1 is coupled to the common node for setting a plurality of Thevenins voltages and Thevenins impedances in response to a plurality of control signals. The Examiner states that the network 30 of *Kim* sets a plurality of

Thevenins voltages and cites elements 31 and 33 of *Kim*. Element 31 of *Kim* is a parallel connection of five field effect transistors (FETs) that are gated ON and OFF with control signals NA0-NA4, respectively. Likewise, Element 33 of *Kim* is a parallel connection of five field effect transistors (FETs) that are gated ON and OFF with control signals NB0-NB4, respectively. *Kim* makes disclosed distinction as to whether the particular FETs in 31 and 33 are N-channel or P-channel devices. *Kim* does not explain clearly the relationship between control signals NA and NB. *Kim* does state that the control signals NA (for element 31) and NB (for element 33) are gated into latch 41 and 43, respectively, from P1UC and P1DC in response to a level of the signal at pad 200. Both latches 41 and 43 are gated with inverters IA and IB which have a common input; therefore, since the latches are the same they are responsive to the same signal at the same signal voltage level. *Kim* never states or implies (See FIG. 2A and FIG. 2B) that whatever number of devices are selected for element 31 are selected for element 33. *Kim* is using active devices with logic levels in his terminator and the Applicants assert the active devices in elements 31 and 33 of *Kim* are not setting Thevenins voltages and Thevenins impedances, as claimed in Claim 1; the active devices characteristics are too variable. Rather, *Kim* is either selecting elements 31 and 33 to either have a high impedance (few devices ON) or low impedance (many devices ON). See *Kim*, column 1, lines 33-53.

Claim 1 of the present invention recites "logic circuitry for generating said plurality of control signals in response to a plurality of mode setting inputs." The Examiner states that PIUC and PIDC is *Kim*'s logic circuitry and that the control signals of *Kim* are generated in response to a plurality of mode setting inputs (signals provided to PIUC and PIDC). Nowhere does *Kim* show PIUC and PIDC receiving mode setting inputs. PIUC and PIDC provide the control signals for 31 and 33 and these signals are gated into latch 41 and 43, respectively, when the signal level at pad 200 reaches a signal level as determined by inverters IA and IB. The best the Applicants can determine, *Kim* turns ON or OFF the same number of selected devices in which case only the impedance would change and not the Thevenins voltage.

A FET acts as a resistor at a particular gate to source voltage (Vgs) only when the voltage across the device drain to source (Vds) is small. As Vds increases (for a give Vgs) a point is reached where the device acts like a current source (current depends on Vgs but not on Vds). Networks 31 and 33 of *Kim* are not designed to act like programmable resistances that set Thevenins voltages and impedances. Rather, the FET devices of *Kim* only act like resistors as the input voltage (pad 200) approaches VDDQ in the case of the up terminator or Ground in the case of his down terminator. For this reason, the Applicants assert that *Kim* is not setting Thevenins voltages and Thevenins impedances, as claimed in Claim 1. Rather, *Kim* is turning ON groups of FETs that have variable characteristics depending on the voltage at pad 200; they act like current sources until the voltage on pad 200 approaches VDDQ or ground at which time they act like resistors whose value is a function of the applied gate to source voltages (NA and NB) control signals. Therefore, the Applicants assert that the rejection of Claim 1 under *35 U.S.C. § 102(b)* as being anticipated by *Kim* is traversed by the above arguments.

Claim 2 is written in independent form and contains all the limitations of Claim 1. Claim 2 adds the limitation that the termination network is comprised of a first and a second termination network, wherein the first termination network sets a Thevenins voltage and Thevenins resistance and the second termination network modifies the Thevenins voltage and Thevenins resistance in response to first and second control signals. The Examiner states that *Kim* teaches the first and second termination networks and cites the multiple FET devices in elements 31 and 33.

The Applicants have shown that elements 31 and 33 do not modify Thevenins voltages and resistances in response to control signals. Rather, the control signals (NA and NB) of *Kim* only turn ON FET devices by applying a gate to source voltage. The specific characteristics of the impedance depends on the voltage at pad 200 (common drain terminal of the FET devices). In the present invention, the termination networks set the Thevenins voltages and resistances only in response to the control signals. The Thevenins voltages and resistances of the termination networks do not depend on the

voltage on the common node (pad 100 or 200) as taught by *Kim*. Therefore, the Applicants respectfully assert that the rejection of Claim 2 under *35 U.S.C. § 102(b)* as being anticipated by *Kim* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 3 is dependent from Claim 2 and contains all the limitations of Claim 1. Claim 2 adds the limitation that a third termination network is coupled to the common node and modifying said Thevenins impedance and said Thevenins voltage in response to third and fourth control signals generated by the logic circuitry. The Examiner rejects Claim 3 by arguing that elements 31 and 33 of *Kim* comprise the third termination network of Claim 3 and the third and fourth control signals are one of *Kim*'s control signals NA and NB and the logic circuitry is PIUC and PIDC. While PIUC and PIDC couple control data to latches 41 and 43, the control signals do not modify elements 31 and 33 until the signal level at pad 200 reaches a level sufficient to turn ON inverters IA and IB. The Applicants have also shown that elements 31 and 33 do not set Thevenins voltages and resistances, rather the outputs of latches 41 and 43 turn ON the FET devices in elements 31 and 33 whose impedance is a function of the voltage level on pad 200. Therefore, the Applicants respectfully assert that the rejection of Claim 3 under *35 U.S.C. § 102(b)* as being anticipated by *Kim* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 4 is dependent from Claim 2 and contains all the limitations of Claim 1. Claim 4 adds the limitation that first termination network is coupled to the common node in response to fifth and sixth control signals generated by the logic circuitry. The Examiner rejects Claim 4 by arguing that the first pull-up transistor and first pull-down transistor of elements 31 and 33 of *Kim* comprise the first termination network of Claim 4 and the fifth and sixth control signals are control signals NA0 and NB0 generated by the logic circuitry. The circuitry of *Kim* couples control data to latches 41 and 43, the control signals do not modify elements 31 and 33 until the signal level at pad 200 reaches a level sufficient to turn ON inverters IA and IB. The Applicants have also shown that

elements 31 and 33 do not set Thevenins voltages and resistances, rather the outputs of latches 41 and 43 turn ON the FET devices (first pull-up transistor and first pull-down transistor) in elements 31 and 33 whose impedance is a function of the voltage level on pad 200. Therefore, the Applicants respectfully assert that the rejection of Claim 4 under *35 U.S.C. § 102(b)* as being anticipated by *Kim* is traversed by the above arguments and for the same reasons as Claims 1 and 2.

Claim 8 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 8 adds the limitation that the receiver circuit is a logic gate having a first logic input coupled to the receiver input and a second logic input coupled to a voltage corresponding to a first logic state, wherein the threshold voltage is a switching voltage of the logic gate and is generated internal to the logic gate. The Examiner states that *Kim* teaches the circuit of Claim 2, wherein the receiver circuit is a logic gate and further states that the receiver 20 of *Kim* is a logic gate. The Applicants assert that the receiver of *Kim* is not a logic gate. *Kim*, in column 6, lines 8-10, states that "according to a preferred aspect of the present invention, the receiver 20 is a comparator and is connected to a reference voltage Vref." A comparator is a high gain circuit that generates an output that is the amplified difference between the voltage at its two inputs; a comparator is not a logic gate having a first logic input coupled to the receiver input and a second logic input coupled to a voltage corresponding to a first logic state, wherein the threshold voltage is a switching voltage of the logic gate and is generated internal to the logic gate as recited by Claim 8. Therefore, the Applicants respectfully assert that the rejection of Claim 8 under *35 U.S.C. § 102(b)* as being anticipated by *Kim* is traversed by the above arguments and for the same reasons as Claims 1 and 2.

Claim 9 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 9 adds the limitation that the receiver circuit of claim 2 is a comparator having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage and a comparator output coupled to said receiver output. The Applicants have shown that *Kim* does not anticipate the circuit of Claim 2, therefore *Kim*

does not anticipate the circuit of Claim 2 with the addition of the comparator of Claim 9. The receiver 20 of *Kim* is not coupled to the same circuitry as Claim 2 and therefore does not anticipate the circuit combination recited in the invention of Claim 9. Therefore, the Applicants respectfully assert that the rejection of Claim 9 under *35 U.S.C. § 102(b)* as being anticipated by *Kim* is traversed by the above arguments and for the same reasons as Claims 1 and 2.

Claim 10 is dependent from Claim 4 and contains all the limitations of Claim 4. Claim 10 adds the limitation that the receiver circuit of Claim 4 is a comparator having a positive input coupled to said input of said receiver, a negative input coupled to said threshold voltage and a comparator output coupled to said receiver output. The Applicants have shown that *Kim* does not anticipate the circuit of Claim 4, therefore *Kim* does not anticipate the circuit of Claim 4 with the addition of the comparator of Claim 10. The receiver 20 of *Kim* is not coupled to the same circuitry as Claim 4 and therefore does not anticipate the circuit combination recited in the invention of Claim 10. Therefore, the Applicants respectfully assert that the rejection of Claim 10 under *35 U.S.C. § 102(b)* as being anticipated by *Kim* is traversed by the above arguments and for the same reasons as Claim 4.

II. REJECTION UNDER 35 U.S.C. § 103(a)

The Examiner rejected Claims 5-7 and 11 under *35 U.S.C. § 103(a)* as being unpatentable over *Kim* in view of U.S. Patent No. 5,739,707 *Barraclough* (hereafter "*Barraclough*").

The Examiner rejected Claims 22-25 and 25-31 under *35 U.S.C. § 103(a)* as being unpatentable over U.S. Patent No. 6,347,350 to *Muljono* (hereafter "*Muljono*") in view of *Kim*.

The Examiner rejected Claims 22-25 and 25-31 under *35 U.S.C. § 103(a)* as being unpatentable over U.S. Patent No. 6,347,350 to *Muljono* in view of *Kim* and further in view of *Barraclough*.

To establish a *prima facie* case of obviousness, the Examiner must meet three basic criteria. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be some reasonable expectation of success. Finally, the prior art reference must teach or suggest all the claim limitations.

Claim 5 is dependent from Claim 4 and contains all the limitations of Claim 4. Claim 5 adds the limitation that the second termination network comprises: a first resistor having a first terminal coupled to a first power supply voltage with a first electronic switch in response to a first logic state of said first control signal and a second terminal and a second resistor having a first terminal coupled to the second terminal of the first resistor and the common node and a second terminal coupled to a second power supply voltage with a second electronic switch in response to a first logic state of the second control signal. The Examiner states that *Kim* teaches all the claimed features of Claim 4 with the exception of teaching the limitations recited in Claim 5. The Examiner states that *Barraclough* teaches the limitations of Claim 5 and cites FIG 4 of *Barraclough* for support of his assertion. The Examiner further states that *Barraclough* teaches in FIG 4, a first resistor (411) having a first terminal coupled to a first power supply voltage (VDD) with a fist electronic switch (401), a second resistor (416) having a first terminal coupled to the second terminal (425) to the first resistor and the common node (415 is a common node) and a second terminal coupled to a second power supply voltage (VSS) with a second electronic switch (406). The Applicants assert first that *Barraclough* is teaching a driver and not a receiver. There is no teaching or suggestion the circuit of *Barraclough* can be used as a receiver. Secondly, the driver of *Barraclough* does not set and modify Thevenins voltages and resistances in response to control signals as claimed in Claim 5. In fact, *Barraclough* points out in column 3, lines 44-54, that the output impedance of the circuit in his FIG 4 is constant when all the resistors have the same value since there is always the same number of resistors in parallel at any time. FIG 4 of *Barraclough* is a driver and not a receiver and it has a constant output impedance rather than an input

impedance (Thevenins impedance of Claim 5) that is modified in response to control signals as claimed in Claim 5. *Barraclough* makes no suggestion or teaching that his driver circuit may be used as a receiver. Likewise, *Barraclough* states that FIG. 4 is an example of an output buffer (driver) that implements a constant impedance voltage source with slew rate limiting. The Examiner states that it would have been obvious to one of ordinary skill in the art at the time of the invention to place resistors, as taught by *Barraclough* (driver circuit), into the circuit of *Kim* (receiver circuit) to provide a receiver circuit having a constant impedance voltage source with slew rate limiting (driver characteristics of *Barraclough*'s driver circuit of FIG. 4). The Examiner, by his own admission, states that the teachings of *Barraclough* when applied to the teachings of *Kim* would result in a receiver circuit with the driver characteristics of the driver in FIG. 4, thus not a receiver at all but rather a driver. The Applicants assert that no one of ordinary skill in the art would look to a circuit that produces a voltage source with constant output impedance and slew rate limiting when designing a receiver with an input impedance set by a termination network that has a Thevenins voltage and impedance that are modified in response to control signals. Therefore, the Applicants respectfully assert that the rejection of Claim 5 under *35 U.S.C. § 103(a)* as being unpatentable over *Kim* in view of *Barraclough* is traversed by the above argument.

The Examiner rejected Claims 6 and 7 for the same reasons as Claim 5. Claim 6 is dependent from Claim 3 and Claim 7 is dependent from Claim 4 and add the same type of limitations to the first and third termination networks that Claim 5 adds to the second termination network. The Applicants have shown that neither *Kim* nor *Barraclough*, singly or in combination, teach or suggest the invention of Claim 5. Therefore, the Applicants respectfully assert that the rejections of Claims 6 and 7, under *35 U.S.C. § 103(a)* as being unpatentable over *Kim* in view of *Barraclough* are traversed by the above argument and for the same reasons as Claim 5.

Claim 11 is dependent from Claim 7 and contains all the limitations of Claim 7. The Applicants have shown that neither *Kim* nor *Barraclough*, singly or in combination,

teach or suggest the invention of Claim 7. Claim 11 adds the limitation that the threshold voltage is equal to one half the difference between said first and second power supply voltages. The Examiner states that neither *Kim* nor *Barraclough*, singly or in combination, teach or suggest this limitation. However, the Examiner states that if the combination of *Kim* and *Barraclough* teaches general conditions of Claim 7, then the limitation of Claim 11 would have been an obvious discovery. The Applicants have shown that *Kim* and *Barraclough*, singly or in combination, do not teach or suggest the invention of Claim 7; therefore, the limitation of Claim 11 is not an obvious extension according to the Examiner's argument. Therefore, the Applicants respectfully assert that the rejection of Claim 11 under *35 U.S.C. § 103(a)* as being unpatentable over *Kim* in view of *Barraclough* are traversed by the above argument and for the same reasons as Claim 7.

Claim 22 is directed to an integrated circuit (IC) having a digital processor, memory for storing instructions and data for the digital processor, input/output (I/O) interface circuitry for communicating to device circuitry external to the IC, a receiver circuit in the interface circuitry for terminating a transmission line coupling the receiver circuit to the device circuitry, wherein the receiver circuit has limitations recited in Claim 1. The Examiner rejects Claim 22 as being unpatentable over *Muljono* in view of *Kim*. The Examiner states that *Muljono* teaches in FIG. 7 a digital processor (702), memory (704 or 706) for storing instructions and data for the digital processor, input/output (I/O) interface circuitry (708 or 710) for communicating to device circuitry external to the IC, a receiver circuit in the interface circuitry for terminating a transmission line (712) coupling the receiver circuit to the device circuitry. The Examiner then states that since *Kim* in FIG. 5 teaches the details of the receiver circuit in the device circuitry recited in Claim 22, that the invention of Claim 22 would be obvious to one of ordinary skill in the art by simply combining the teachings of *Muljono* and *Kim*. The Applicants have shown that *Kim* does not teach or suggest the receiver circuitry of Claim 1. The Examiner makes no assertion that *Muljono* teaches or suggests the receiver circuit of Claim 1. Therefore, the Applicants assert that *Muljono* and *Kim*, singly or in combination, do not

teach or suggest the receiver circuit of Claim 1. The Applicants, therefore, respectfully assert that *Muljono* and *Kim*, singly or in combination, do not teach or suggest the IC of Claim 22 that contains the receiver circuit of Claim 1. Therefore, the Applicants assert that the rejection of Claim 22 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* is traversed by the above argument and for the same reasons as Claim 1.

Claim 23 is an independent claim that contains all the limitations of Claim 22 and adds the limitation that the termination network comprises a first termination network coupled to the common node for setting a Thevenins impedance and a Thevenins voltage at said common node and a second termination network coupled to the common node for modifying the Thevenins impedance and the Thevenins voltage in response to first and second control signals. Claim 23 adds the same limitation to the IC of Claim 22 that Claim 2 adds to the receive circuit of Claim 1. The Examiner states that *Muljono* teaches the IC of Claim 22 and *Kim* teaches the receiver circuit of Claim 22. Further, the Examiner states that *Kim* teaches the limitations of the receiver circuit in Claim 23 which are the same as the limitations of the receiver circuit of Claim 2. The Applicants have shown that *Kim* does not teach or suggest the receiver circuit of Claim 2. Likewise, the Examiner makes no assertion that *Muljono* teaches or suggests the receiver circuit of Claim 2 and Claim 23. Therefore, the Applicants assert that *Muljono* and *Kim*, singly or in combination, do not teach or suggest the IC of Claim 23 with the receiver circuit having the limitations of the receiver circuit of Claim 1. Therefore the Applicants assert that the rejection of Claim 23 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* is traversed by the above argument and for the same reasons as Claims 1 and 22.

Claim 24 is dependent from Claim 23 and contains all the limitations of Claim 22. Claim 23 adds the same limitations to Claim 23 as Claim 3 adds to Claim 2. The Applicants have shown that *Kim* does not teach or suggest the invention of Claim 3. Likewise, the Examiner makes no assertion that *Muljono* teaches or suggests the receiver

circuit of Claim 3 and Claim 24. Therefore, the Applicants assert that *Muljono* and *Kim*, singly or in combination, do not teach or suggest the IC of Claim 24 with the receiver circuit having the limitations of the receiver circuit of Claim 3. Therefore, the Applicants assert that the rejection of Claim 24 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* is traversed by the above argument and for the same reasons as Claims 3 and 23.

Claim 25 is dependent from Claim 23 and contains all the limitations of Claim 23. Claim 25 adds the same limitations to Claim 23 as Claim 4 adds to Claim 2. The Applicants have shown that *Kim* does not teach or suggest the invention of Claim 4. Likewise, the Examiner makes no assertion that *Muljono* teaches or suggests the receiver circuit of Claim 4 and Claim 25. Therefore, the Applicants assert that *Muljono* and *Kim*, singly or in combination, do not teach or suggest the IC of Claim 25 with the receiver circuit having the limitations of the receiver circuit of Claim 4. Therefore, the Applicants assert that the rejection of Claim 25 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* is traversed by the above argument and for the same reasons as Claims 3 and 23.

Claim 29 is dependent from Claim 23 and contains all the limitations of Claim 23. Claim 29 adds the same limitations to Claim 23 as Claim 8 adds to Claim 2. The Applicants have shown that *Kim* does not teach or suggest the invention of Claim 9. Likewise, the Examiner makes no assertion that *Muljono* teaches or suggests the receiver circuit of Claim 8 and Claim 29. Therefore, the Applicants assert that *Muljono* and *Kim*, singly or in combination, do not teach or suggest the IC of Claim 29 with the receiver circuit having the limitations of the receiver circuit of Claim 9. Therefore, the Applicants assert that the rejection of Claim 29 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* is traversed by the above argument and for the same reasons as Claims 8 and 23.

Claim 30 is dependent from Claim 23 and contains all the limitations of Claim 23. Claim 30 adds the same limitations to Claim 23 as Claim 9 adds to Claim 2. The

Applicants have shown that *Kim* does not teach or suggest the invention of Claim 9. Likewise, the Examiner makes no assertion that *Muljono* teaches or suggests the receiver circuit of Claim 9 and Claim 30. Therefore, the Applicants assert that *Muljono* and *Kim*, singly or in combination, do not teach or suggest the IC of Claim 30 with the receiver circuit having the limitations of the receiver circuit of Claim 9. Therefore, the Applicants assert that the rejection of Claim 30 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* is traversed by the above argument and for the same reasons as Claims 9 and 23.

Claim 31 is dependent from Claim 23 and contains all the limitations of Claim 23. Claim 31 adds the same limitations to Claim 23 as Claim 10 adds to Claim 2. The Applicants have shown that *Kim* does not teach or suggest the invention of Claim 10. Likewise, the Examiner makes no assertion that *Muljono* teaches or suggests the receiver circuit of Claim 10 and Claim 31. Therefore, the Applicants assert that *Muljono* and *Kim*, singly or in combination, do not teach or suggest the IC of Claim 31 with the receiver circuit having the limitations of the receiver circuit of Claim 10. Therefore, the Applicants assert that the rejection of Claim 31 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* is traversed by the above argument and for the same reasons as Claims 10 and 23.

Claim 26 is dependent from Claim 25 and contains all the limitations of Claim 25 and Claim 23. Claim 23 is an independent claim that contains all the limitations of Claim 22. The Examiner states that *Muljono* in view of *Kim* teaches all the claimed features of the IC in Claim 22. The Applicants have shown that *Muljono* in view of *Kim* does not teach or suggest, singly or in combination, the invention of Claim 22. The Examiner states that *Muljono* in view of *Kim* does not teach or suggest, singly or in combination, the invention of Claim 26. However, the Examiner states that *Barraclough* teaches in FIG. 4, a first resistor (411) having a first terminal coupled to a first power supply voltage (VDD) with a fist electronic switch (401), a second resistor (416) having a first terminal coupled to the second terminal (425) to the first resistor and the common

node (415 is a common node) and a second terminal coupled to a second power supply voltage (VSS) with a second electronic switch (406).

The Applicants first assert that *Barraclough* is teaching a driver and not a receiver. There is no teaching or suggestion that the circuit of *Barraclough* can be used as a receiver. Secondly, the driver of *Barraclough* does not set and modify Thevenins voltages and resistances in response to control signals as claimed in Claim 5. In fact, *Barraclough* points out in column 3, lines 44-54, that the output impedance of the circuit in his FIG. 4 is constant when all the resistors have the same value since there is always the same number of resistors in parallel at any time. FIG. 4 of *Barraclough* is a driver and not a receiver and it has a constant output impedance rather than an input impedance (Thevenins impedance of Claim 5) that is modified in response to control signals as claimed in Claim 5. *Barraclough* makes no suggestion or teaching that his driver circuit may be used as a receiver. Likewise, *Barraclough* states that FIG. 4 is an example of an output buffer (driver) that implements a constant impedance voltage source with slew rate limiting. The Examiner states that it would have been obvious to one of ordinary skill in the art at the time of the invention to place resistors, as taught by *Barraclough* (driver circuit), into the circuit of *Kim* (receiver circuit) to provide a receiver circuit having a constant impedance voltage source with slew rate limiting (driver characteristics of *Barraclough*'s driver circuit of FIG. 4). The Examiner, by his own admission, states that the teachings of *Barraclough* when applied to the teachings of *Kim* would result in a receiver circuit with the driver characteristics of the driver in FIG. 4, thus not a receiver at all but rather a driver. The Applicants assert that no one of ordinary skill in the art would look to a circuit that produces a voltage source with constant output impedance and slew rate limiting when designing a receiver with an input impedance set by a termination network that has a Thevenins voltage and impedance that are modified in response to control signals. Therefore, the Applicants respectfully assert that the rejection of Claim 26 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* and further in view of *Barraclough* is traversed by the above argument and for the same reasons as Claims 5 and 23.

Claim 27 is dependent from Claim 24 and Claim 28 is dependent from Claim 25. The Examiner states that Claims 27 and 28 are rejected for the same reasons as Claim 26. Therefore, the Applicants respectfully assert that the rejection of Claims 27 and 28 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* and further in view of *Barraclough* are traversed for the same reasons as Claims 5, 23 and 26.

Claim 32 is dependent from Claim 28 and contains all the limitations of Claim 28. The Examiner states that *Muljono* in view of *Kim* and further in view of *Barraclough* does not teach or suggest, singly or in combination, the invention of Claim 32. However, the Examiner states that since he believes *Muljono* in view of *Kim* and further in view of *Barraclough* does teach the invention of Claim 28, that the limitation of Claim 32 would have been obvious. The Applicants reject this assertion as the Applicants have shown that *Muljono* in view of *Kim* and further in view of *Barraclough* does not teach or suggest, singly or in combination, the invention of Claim 28. The Applicants further assert that the Examiner has not made a *prima facie* case that the general conditions of Claim 28 is disclosed in the prior art. Therefore, the Applicants respectfully assert that the rejection of Claim 32 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* and further in view of *Barraclough* are traversed for the same reasons as Claims 5, 23 and 28.

IV. CONCLUSION

The Applicants have traversed the objections of Claims 9 and 10 because of supposed informalities.

The Applicants have traversed the rejection of Claims 5-7 and 26-28 under *35 U.S.C. § 112*, second paragraph, as being indefinite by amending Claims 5-7 and 26-28.

The Applicants have traversed the rejections of Claims 1-4 and 8-10 under *35 U.S.C. § 102* as being anticipated by *Kim*.

The Applicants have traversed the rejections of Claims 5-7 and 11 under *35 U.S.C. § 103(a)* as being unpatentable over *Kim* in view of *Barraclough*.

The Applicants have traversed the rejections of Claims 22-25 and 29-31 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim*.

The Applicants have traversed the rejections of Claims 26-28 and 32 under *35 U.S.C. § 103(a)* as being unpatentable over *Muljono* in view of *Kim* and further in view of *Barraclough*.

The Applicants, therefore, respectfully assert that Claims 1-42 are now in condition for allowance and request an early allowance of these claims.

Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,

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